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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/067,599
Filing Date: April 28, 1998
Appellant(s): ALLISON ET AL.

Joscelyn G. Cockburn

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 19 April 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief, page 1 is correct.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief, page 2.

(3) Status of Claims

The present application is a CPA

Claims 1-14 have been canceled, paper no. # 9.

Claims 15-20, 33, 36-38 are remain rejected as follows:

Claims 15-16, 19-20, 33 and 36 are rejected under 35 US.C. 102(e) as being anticipated by Dosiere et al., [hereafter Dosiere], US Patent No. 577800.

Claims 17-18, 37-38 rejected under 35 USC 103(a) as being unpatentable over Dosiere et al. [hereafter Dosiere], US Patent No. 577800 as applied to Claims 15,19 above, and further in view of Jeng, US Patent No. 5892768.

After further consideration based on the arguments in the page 7, 9-22, rejection of independent Claim 21 and 34 are dropped, Claims 22-32 are dependent on Claim 21, Claim 35 is dependent on Claim 34 are also dropped.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

The present invention is directed to a mechanism that uses pattern matching to provide the wake-up function to devices in a network. The closest prior art Jeng, US Patent No. 5,892,768 teaches transmitting over the Ethernet a frame or packet that contains series of bits forming a complete unit of information that is sent across a network, especially Ethernet MII [see Abstract]. However, Jeng either singularly or in combination, fail to anticipate or render obvious the recited feature in Claim 21 *"a network interface circuit arrangement", "a pattern match logic circuit arrangement correlating marked patterns in said first storage with the data and generating at least one first control signal if a match occurs between one of the marked patterns and the data"*. These features together with the other limitations of the independent claims are novel and non-obvious over the prior art of record. The dependent Claims 22-32 being definite, enabled by the specifications, and further limiting to the independent clam, are also allowable.

The present invention is directed to a mechanism that uses pattern matching to provide the wake-up function to devices in a network. The closest prior art Williams et al. US Patent No. 5938771 teaches network interface for generating a power management wake up signal to initiate a wake-up routine of a host computer

comprises remote wake up request signal in response to detecting a wake up request in a received data packet from a network [see Abstract, col 2, line 24-39]. However, Williams either singularly or in combination, fail to anticipate or render obvious the recited feature in Claim 34 "*correlating each identified pattern with data received from the communications network; and generating a wake-up signal if a match occurs in step (c)".* These features together with the other limitations of the independent claim are novel and non-obvious over the prior art of record. The dependent Claim 35 being definite, enabled by the specifications, and further limiting to the independent claim, is also allowable.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief page 2 is correct.

(5) Summary of Invention

The summary of invention contained in the brief page 2-3 is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that Group I includes claims 15-16, 19-20,33 and 36, Group II includes Claims 33-34, and Group III includes Claims 17-18, 21-22 and 37-38 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief pages 24-28 is correct.

(9) Prior Art of Record

5,778,000	Dosiere et al	7-1998
5,938,771	Williams et al	8-1999
5,892,768	Jeng	4-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 15-16, 19-20, 33 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Dosiere et al., [hereafter Dosiere], US Patent No. 577800.

2. As to Claims 15,19, and 33, Dosiere details a system which including 'a first memory in which a set of patterns are stored' [col 2, line 4-5, col 4, line 47-48, col 5, line 20-22, col 10, line 22-23], examiner notes that Dosiere uses first m-bit set are in the first memory, fig 3a represents part of the first memory, see col 7, line 38-39, 'a second memory' [col 2, line 7-9, col 5, line 20-22], Dosiere specifically details first memory and second memory, containing m-bit set forms n-bit pattern bits, 'identifying patterns in the first memory to be matched against the data' [col 1, line 62-67, col 4, line 56-64], Dosiere's teachings including bit-by-bit comparison, examiner interpreting matching data to be equivalent to Dosiere's including bit-by-bit comparison, 'mask data' [col 2, line 46-60]; 'pattern match logic circuit arrangement correlating marked patterns in said first memory against the data ' [col 5, line 20-37].

3. As to Claims 16 and 20, Dosiere details a system which including 'marked patterns are fewer than the total number of patterns in said first memory' [col 4, line 54-61].

4. As to Claim 36, Dosiere details a system, which includes 'pointers include mask bits' [col 6, line 27-29, line 49-52, see fig 2a-2b, 3a-3b].

5. Claims 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al., [hereafter Williams], US Patent No. 5938771.

6. As to Claim 33, Williams details a system which including 'pattern matching or providing a set of patterns' [fig 2, element 60, col 4, line 50-53], examiner interpreting pattern matching or providing a set of patterns are to be equivalent to Williams fig 2, element 60 because it associated with Pattern Match signal from the pattern match logic, element 60, see col 4, line 56-57; 'providing data to be matched with selected patterns' [col 4, line 56-62], 'providing pointers for identifying the selected patterns' [col 5, line 31-42, line 43-50], examiner interpreting pointers are inherent aspect of Williams because firstly Williams teachings including read/write operations depended on the bit status from the register 76a, secondly, Magic Packet logic element 62 has the ability to scan incoming frames with specific addresses as detailed in col 5, line 43-45, thirdly, pointer(s) is a variable that simply contains the memory location or memory address of some data rather than the data itself, and address is specifying a location in the memory where data is stored is well known in the art; 'correlating the data with the selected patterns' [col 6, line 4-13], 'generating a match signal if the data and the selected patterns match' [col 6, line 25-44].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 17- 18, 37-38 rejected under 35 U.S.C. 103(a) as being unpatentable over Dosiere et al., [hereafter Dosiere], US Patent No. 5778000 as applied to claim15, 19 above, and further in view of Jeng, US Patent No. 5892768.

8. As to Claim 17 Dosiere do not specifically teach 'data is received from a network', although Dosiere teaches data manipulation between first and second memory [see col 5, line 21-23]. Jeng details a system which including 'data is received from a network' [col 2, line 13-17, col 2, line 41-44], more specifically, Jeng teaches Ethernet media independent interface, see fig 2.

It would have been obvious one of the ordinary skill in the art at the time of the applicant invention to combine the concepts taught by Jeng with the system of Dosiere because receiving data from a network allows access to much more information than access in local memory of Dosiere [see Dosiere, col 7, line 38-39 a second memory col 2, line 7-9, col 5, line 20-22] and thus improving the communication of computer data in a network more specifically store and forward [col 1, line 45-49].

9. As to Claim 18, Jeng teaches a system which including 'first state machine for assembling data received from a network into predetermined sizes' [col 2, line 41-46], examiner interpreting predetermined sizes to be equivalent to Jeng's 4-bit data packets converted into 8-bit data packets [see fig 5B]; Dosiere teaches ' identifying beginnings and endings of data frames' [col 5, line 56-59], 'a second state machine operatively coupled to the first state machine' [col 1, line 45-47], 'second state machine including circuit that receives the predetermined sizes from the first state machine' [col 2, line 11-25], although generating addresses for accessing the first and second memory are inherent aspect of Jeng's teachings because Jeng specifically teaches for example

buffer memory, see fig 2, elements 50, and 52, more specifically, Dosiere teaches addresses for accessing data, see fig 3a, col 7, line 38-47; 'pattern and mask data are to be read and used with the predetermined sizes in generating the first control signal' [see fig 4, col 8, line 39-67, col 9, line 1-7]

10. As to Claim 36, Dosiere teaches patterns and mask data [see fig 1, col 2, line 61-67, col 3, line 1-27, col 4, line 26-29], specifically, m-bit set forms part of n-bit pattern [see col 2, line 55-50, col 5, line 43-48, line 65-67], examiner notes that Dosiere suggests extracting a first set of "m" bits from the bit stream [see col 1, line 43-45], also suggests extracting second set of bits [see col 1, line 488-51], in general, Dosiere teaches m-bit set form part of the n-bit pattern [see col 4, line 56-58], therefore, n-bit pattern would have include eight patterns.

11. As to Claim 37, Dosiere teaches '32-bit with groups of 4 mask bits identifying one of the eight patterns' [col 6, line 42-48].

(11) Response to Argument

12. At page 4, item A, Dosiere does not teach two(2) memories, at page 5, line 1-5, This and other statements in Dosiere clearly supports Appellant's position that Dosiere only discloses a single memory. Claims 15,16,19, and 20 calls for – first memory –; second memory... As argued above Dosiere teaches only a single memory.

Examiner disagree to this contention because Dosiere does have more than one memory for example Dosiere specifically teaches first memory includes a first pointer to a second memory location being a first entry of a linked list, further second memory location including information about n-m bits of the n-bit pattern [see col 2, line 5-10], therefore, the elements of Claims 15-16, 19-20 are rejected based on the Dosiere's prior art.

13. At page 5, item B, Dosiere does not teach mask data identifying patterns to be matched, page 5, line 15-16, mask data identifying patterns to be matched against data (Claims 15-16, 19-20).

Examiner disagree with the applicant because firstly, Dosiere's teachings including head mask pattern indicating bit position [see col 2, line 41-43], secondly, particular Dosiere also teaches for example indicated bit position is followed by the bit-value [see col 2, line 44-47]. Dosiere further suggests head mask pattern indicating

which bit position to be verified in m-bit set, first set of the bit-values being a tail match pattern [see col 2, line 47-55], Dosiere's teachings including n-bit for which a bit-by-bit comparison of first m-bit set with consecutive bits contained with the n-bit pattern, see col 1, line 62-67, col 2, line 1-4.

14. At page 5, lines 16-17, Appellants contend Dosiere does not teach providing a set of patterns...(Claims 15,16,19,20,33 and 36).

Examiner disagree with the applicant because firstly Dosiere specifically teaches detection of an n-bit pattern in a bit stream as detailed in Abstract, secondly, Dosiere teaches bitstream position based on n-bit pattern as detailed in col 5, line 12-22], thirdly, Dosiere teaches various patterns, more specifically head match pattern, tail mask pattern as detailed in col 5, line 25-46.

15. At page 5, line 17, Appellants contends Dosiere does not teach providing pointers for identifying the selected patterns.

Examiner disagree with the applicant because Dosiere specifically directed to part of the first memory contents such as shown in fig 2a, part of the linked list entries such as shown in fig 2b locations denoted by the pointer value such as 0001 as detailed in col 6, line 49-52. As best understood by the Examiner, pointer is a variable that contains the memory location address of some data rather than the data itself.

16. At page 6, line 5-6, Dosiere does not teach mask data to identify the patterns to be matched against data.

Examiner disagree with the applicant because firstly, Dosiere directed to various mask pattern, more specifically head mask pattern, tail mask pattern, as detailed in col 5, line 25-37, further Dosiere also directed to for example head mask pattern, indicating the positions of bits, while head match pattern containing the values that the bits in the position indicated by the head mask pattern should match with as detailed in col 5, line 28-30.

17. At page 7, item D, Claim 33, line 4, Williams fails to teach the details of any pattern matching techniques.

Examiner disagrees with the applicant because Williams teaches for example pattern match logic, fig 2, element 60 also known as PMAT, more specifically Williams directed to Magic Packet™ match logic 62 for detecting a wake up request in a received packet from the MAC 20 as detailed in col 4, line 50-54. It is however, noted from the Williams background Magic Packet™ is simple because the associated logic is looking for specific pattern for matching within the data packets as detailed in col 1, line 47-52.

18. At page 8, line 1-4, Appellants find this portion of the examineer's.....

As to the above argument: Examiner rejected independent Claim 33 based on the prior art Dosiere et al., US Patent No. 577800 [see paper no. # 13, page 3], also Examiner given another rejection of independent Claim 33 based on the prior art Williams, US Patent No. 5938771 [see paper no. # 13, page 4]. The Claim 36 is dependent on Claim 33 is rejected based on the prior art Dosiere et al. US Patent No. 577800 [see paper no. # 13, page 3-4]. Claims 37-38 are rejected under 35 103(a) prior art Dosiere et al in view of Jeng, US Patent No. 5892768., since Claim 36 is rejected based on the prior art Dosiere et al., US Patent No. 577800.

19. At page 14, item V, line 11-13, the references not teaching two memories with one storing patterns and one storing mask bits to identify patterns to be matched the references do not teach first state machine and second state machine performing functions

As to the above argument Dosiere specifically teaches two memories, more specifically first memory includes a first pointer to a second memory location being a first entry of a linked list, further second memory location including information about n-m bits of the n-bit pattern as detailed in col 2, line 5-10, further Dosiere teaches first set of bit values being a head match pattern. Examiner in the rejection, Jeng teaches

specifically teaches first state machine and second state machine as detailed in col 2, line 41-46, col 2, line 11-25 respectively..

20. At page 20, item N, line 12-13, Claim 36 calls for pointers which are mask bits to identify patterns within the pattern RAM. Dosiere does not teach this feature.

Examiner disagrees with the applicant because Dosiere specifically teaches pointers which are mask bits identifying patterns as detailed in fig 2a-2b. Dosiere directed to for example memory location contains a bit pointer, and its values, setting a match for 16-bit memory location further contains a head mask pattern with a value as detailed in col 7, line 13-19.

21. At page 21, item O, line 10-11, Dosiere does not teach 32-bit groups of 4 mask bits identifying one of the eight patterns.

As to the above argument, Dosiere specifically teaches for example hexadecimal code used in which frameword has a length of 32-bit, each hexadecimal code represents 4-bits, further indicates the n-bit pattern as detailed in col 6, line 42-48.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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May 2, 2002

Conferees

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